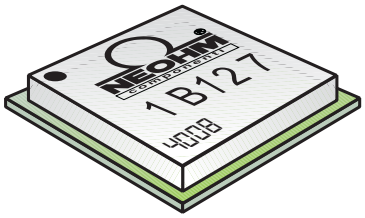
MCM

Latch-Up and Overcurrent Protection System



1B127

FEATURES

- Wide Supply voltage range: 2.7 – 36V
- Low power consumption
- Maximum current: 2 A
- Programmable current threshold
- Only one external resistor required
- Wider voltage and current range with external transistor
- Load disable input
- Current monitor output
- Programmable off time *(with external capacitor)*
- Filters out inrush current *(with external capacitor)*
- Controlled slew-rate *(with external capacitor)*
- Guaranteed radiation tolerance up to 30krad TID
- Wide temperature range: –40°C to +125°C

APPLICATIONS

- Latch-up monitoring and protection systems
- Overcurrent protection
- Load switch with over-current monitoring
- Load switch with slew-rate limitation
- Protects low-cost devices from latch-ups

DESCRIPTION

Latch-up is a catastrophic phenomenon which affects CMOS devices. It is caused by high energy particles or ionizing radiations or other causes which trigger the parasitic transistors, mostly in CMOS devices that are not radiation-hardened.
The 1B127 is a latch-up and overcurrent protection system suited for high radiation level environments, such as Low Earth Orbit satellites.

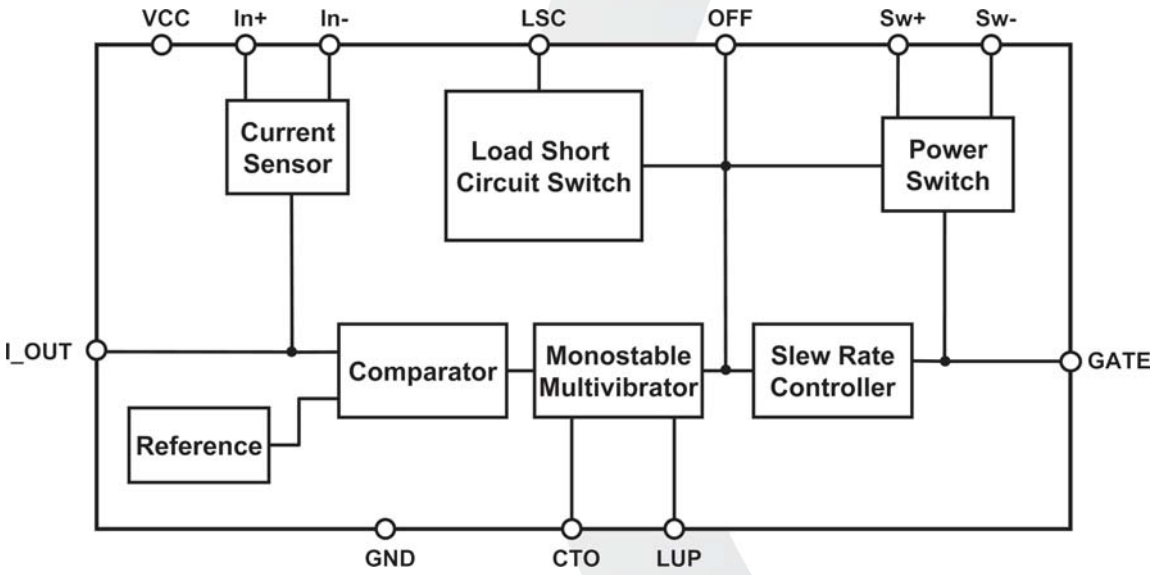


Figure 1. Block diagram.

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UNI EN ISO 9001: 2000

It allows using low-cost devices (COTS) in radiation environments like space applications, high-energy physics experiments and biomedical equipment, by protecting them against the effects of latch-up. The system monitors the current flowing through an external sense resistor (Rs) and whenever a threshold value is reached the internal pass transistor switches off the load. After a user-defined recovery time, the pass transistor automatically turns on again restoring power supply to the load, once the latch-up has faded away.
The device can also be used as a current-limited load switch by sending a TTL signal to the OFF pin. For higher voltages or currents, an external PMOS pass transistor can be used.
Inrush current effects or short current spikes can be filtered away. Allowed inrush charge and recovery time can be set using external capacitors.
In addition, the slew-rate while turning on load supply voltage can be limited using an external capacitor to program the inrush current.
The device is available in a small 13x13 mm plastic 100BGA package and it is available for the extended temperature range (-40 °C to +125 °C). It has a low quiescent current, which makes it suitable for low power systems.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (VAL)	-0.3V ÷ 36V
Analog Input Vin+ , Vin-	Vcc-0.3V÷Vcc+0.3V
Differential voltage	-40V ÷ 2V
OFF input	-0.3V ÷ 36V
Internal Load Switch Max V	18V
Load Curr. with Internal Switch	2A
Max current sink	300mA
Operating Temperature	-40°C ÷ +125°C
Storage Temperature	-50°C ÷ +150°C
Junction Temperature	+150°C

OPERATION

The 1B127 device (see block diagram in fig. 1) monitors the current on the high side by measuring the differential voltage across a shunt resistor (pins IN+ and IN-).
The floating differential voltage is transformed into a ground-referenced voltage on the I_OUT pin. An external capacitor connected to the I_OUT pin allows filtering short current spikes, while an external resistor connected to the same pin allows changing the gain of the current monitor.
A comparator detects when the current overpasses a threshold value, triggering a monostable for a fixed time period. An external capacitor across pins CTO and LUP allows to increase that time period.
The output of the monostable (which is available as a logic signal on the LUP pin) turns off the internal power switch (across SW+ and SW- pins), disconnecting the load from the power supply. An additional output LSC optionally sinks current from the load, when load supply is removed, to discharge capacitors which might be present on the load or to sink leakage currents which might come from other input/output connections of the load.
After the monostable resets to its normal condition, the power switch is turned on again to supply power to the load. The slew-rate controller optionally limits

The OFF pin may optionally turn load power off under user control.
The control of the power switch is also available via the GATE pin to drive an external power transistor, augmenting load voltage or load current capabilities.

Figure 2 shows the basic configuration of the circuit,

$$R_S = \frac{V_{th}}{I}$$

Where I is the current through the sense resistor (that is, load current), and Vth is the device threshold voltage. The power rating of this resistor shall be at least:

$$P_{R_S} = \frac{V_{th}^2}{R_S}$$

The I_OUT voltage can be calculated as:

$$V_{I\_OUT} = I \cdot R_S \cdot Gain$$

where nominal Gain without ext components is 30.

The Gain can be modified (together with threshold voltage) as shown in fig. 3, by adding an external resistor Rth:

$$R_G = \frac{R_{th} R_{OUT}}{R_{th} + R_{OUT}}$$

$$Gain = \frac{R_G}{5k\Omega}$$

$$V_{th} = \frac{600mV}{Gain}$$

where ROUT is the output impedance of the I_OUT output (nominal value 150k).

By adding the CIR capacitor, as shown in Figure 3, the I_OUT is filtered by a low-pass filter with cut-off frequency of:

$$f_T = \frac{1}{2\pi (C_{IR} + 100pF) \cdot R_G}$$

allowing an inrush charge without triggering of:

$$Q = \frac{(C_{IR} + 100pF) \cdot 3kV\Omega}{R_S}$$

Adding the CTC capacitor, as shown in Figure 3, the recovery time can be increased according to the following equation:

$$C_{TC} = \frac{T_{OFF}}{100k\Omega} - 100nF$$

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To control the slew-rate of load voltage to prevent high inrush currents into the load, an external capacitor (C_{SR} in Figure 3) can be used and its value is given by:

$$C_{SR} = \frac{T_{rise} - 165us}{33k\Omega}$$

In more than 2A or more than 18V supply voltage are needed, an external PMOS pass transistors can be used (as shown in Figure 4). The external pass transistor is driven by the SW+, SW- and GATE pins shorted together.
In this case the CSR capacitor should be calculated according to the following equation (CG is the external PMOS gate capacitance):

$$C_{SR} = \frac{T_{rise}}{3.3 \cdot 10^4 \Omega} - C_G$$

Adding an external diode and transistor as shown in fig. 5, locks the the monostable in this way, once the device has been triggered by an overcurrent, only turning the external MOS on resets the 1B127 device to its normal operation.

Figure 6 shows a fault-tolerant configuration where a pair of 1B127 devices are paralleled to increase fault tolerance. A short circuit on one of the pass transistors (internal or external) and a stuck-open fault on the 1B127 mos driver can be tolerated. In case of stuck-closed on the 1B127 driver the latch-up protection is no more effective but the load can still be turned on.

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ELECTRICAL CHARATERISTICS

All characteristics at T_A= 25 °C, V_{CC} = 5 V, unless otherwise noted. $^*V_{sense}$= V_{in+} - V_{in-}*

Parameter	Condition	1B127			Unit
		Min	Typ	Max	
INPUT					
Differential Input Voltage			20	500	mV
Common-Mode Input Range		Vcc -100mV	Vcc	Vcc +100mV	V
Common-Mode Rejection	V_{in+} = 2.7 V to 30 V, V_{sense} = 20 mV (*)	100	120		dB
Threshold voltage V_{th}	without external components	29	30	31	mV
over temperature range		28		32	mV
temperature drift			1		µV / °C
drift vs. common mode (V_{in+})	V_{in+} = 2.7 V to 36 V		0.04	4	µV / V
Input Bias Current			2		µA
over temperature range				10	µA
POWER SUPPLY					
Supply Voltage	Vcc	2.7		36	V
Supply Current	Vcc = 3 V			200	µA
	Vcc = 5 V			360	µA
	Vcc = 15 V			700	µA
	Vcc = 36 V			2	mA
POWER SUPPLY					
Continuous Load Current				2	A
Peak Load Current	1 ms pulses, DC < 1%			3	A
Supply Voltage		2.7		20	V
Leakage Current	-40 °C < T_A < 125 °C			100	µA
TIMING					
Turn-off time:	Inrush current = 2 I_{th}			100	µs
	C_{IR} = 0				
	C_{IR} = 2.7 nF			1	ms
Recovery Time	without external components		10		ms
	C_{TC} = 1 nF		110		ms
SINK CURRENT					
Sink Current	Vcc = 2.7 V	5			mA
	Vcc = 15 V ÷ 36 V			36	mA
Peak Current	1 ms pulses, DC < 1%			500	mA
I_OUT					
Gain, without external components		29	30	31	
	over Temperature	28	30	32	
Output Impedance R_{out}			150		KΩ
Output Swing			0.6		V
THERMAL					
Thermal Resistance between power switch junction to balls	Thermal Resistance θ_{JC}		12		°C / W
Thermal Resistance between power switch junction to ambient	Thermal Resistance θ_{JA} Mounted on std 1.6mm PCB		34		°C / W
ESD					
All Pins	HBM 1.5KΩ, 100pF	2			KV

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APPLICATION DIAGRAMS

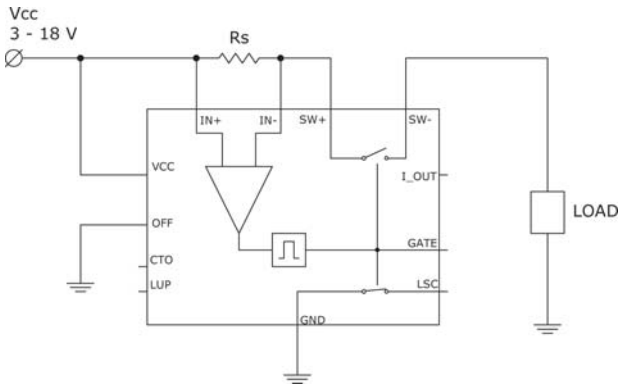

Figure 2. Basic device configuration.

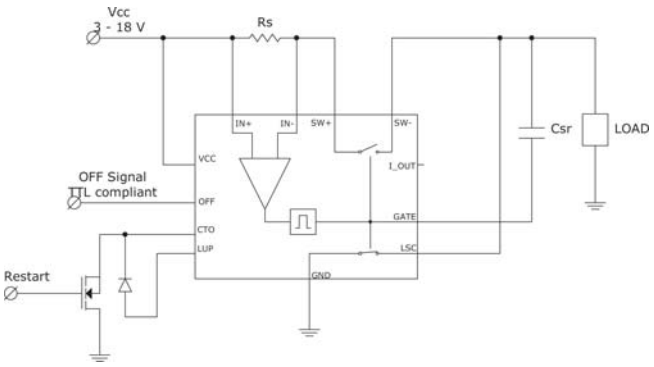

Figure 5. Current protection with restart signal.

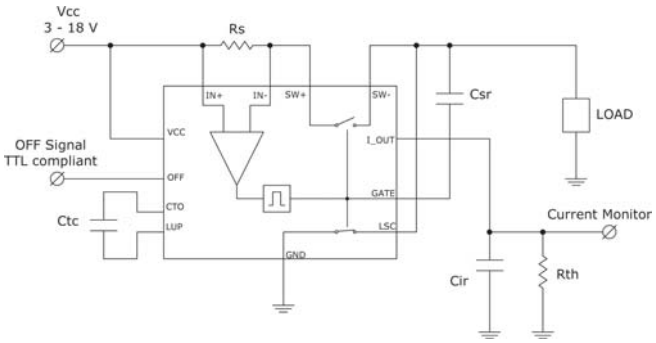

Figure 3. Circuit with T_{OFF} and Slew-Rate control.

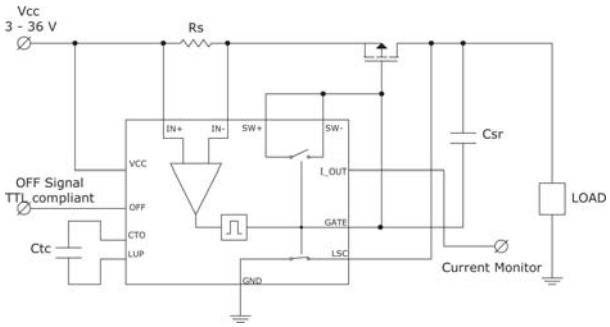

Figure 4. Circuit with an external Pass Transistor to increase load current.

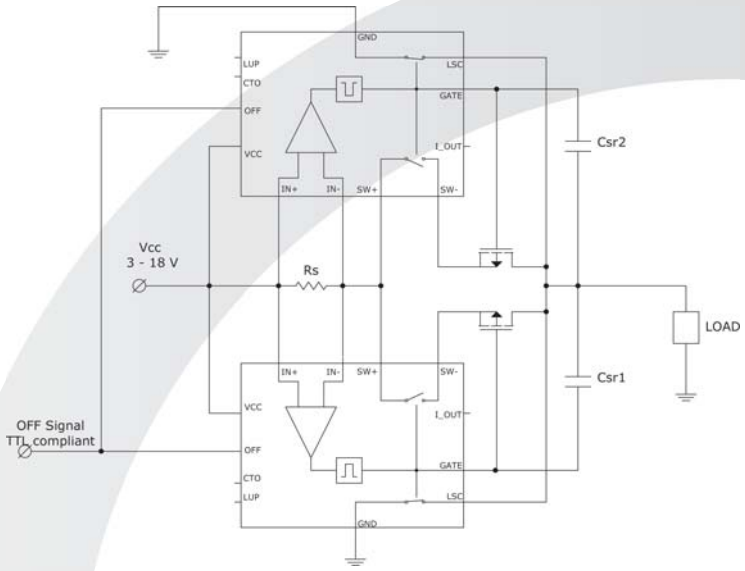

Figure 6. Fault-tolerant configuration with two parallel branches and two series transistors.

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TYPICAL CHARACTERISTICS

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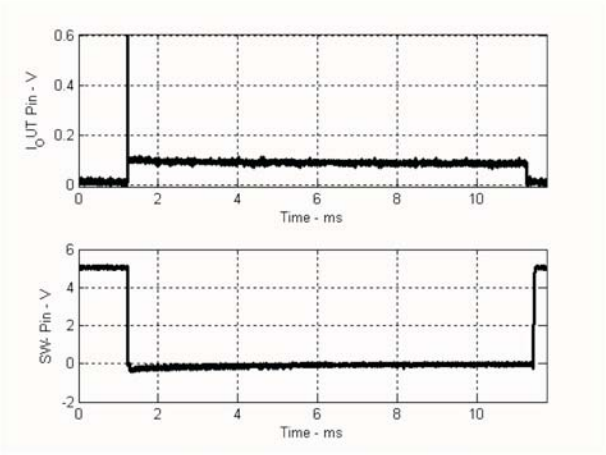

Figure 7. Latch-up event with V_{CC} = 5 V.

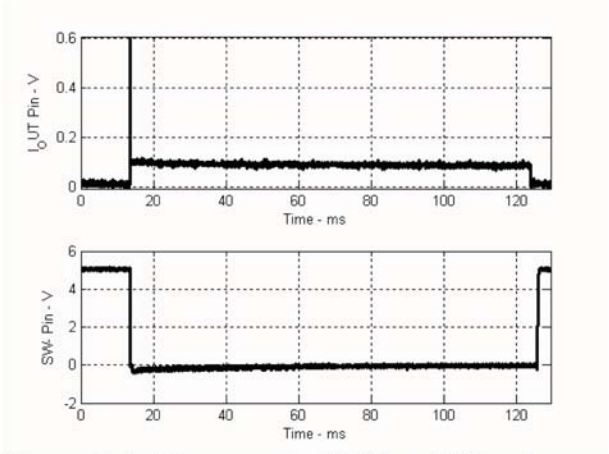

Figure 8. Latch-up event with V_{CC} = 5 V and C_{TC} = 1 uF.

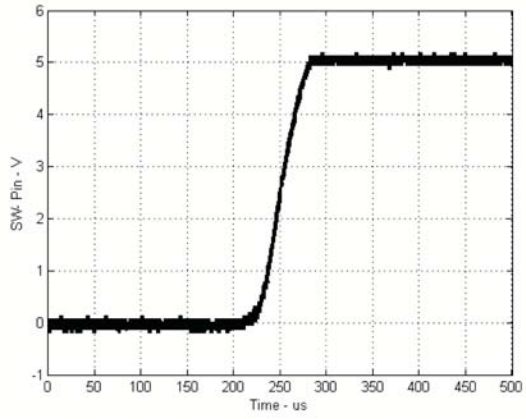

Figure 9. Turn-on time with V_{CC} = 5 V and no external component.

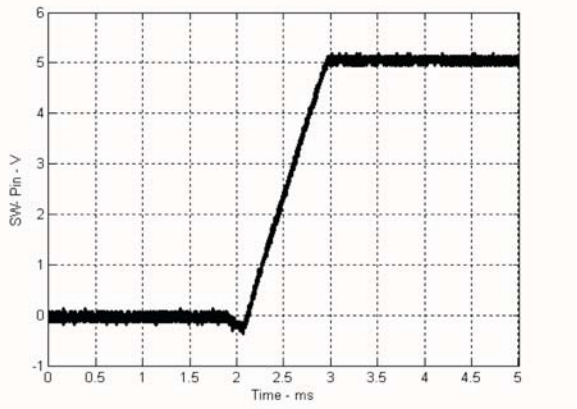

Figure 10. Limited slew-rate with V_{CC} = 5 V and C_{SR} = 2.7 nF.

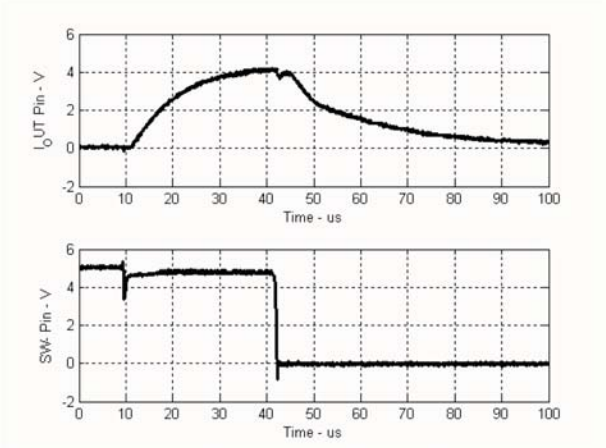

Figure 11. Turn off time with V_{CC} = 5 V.

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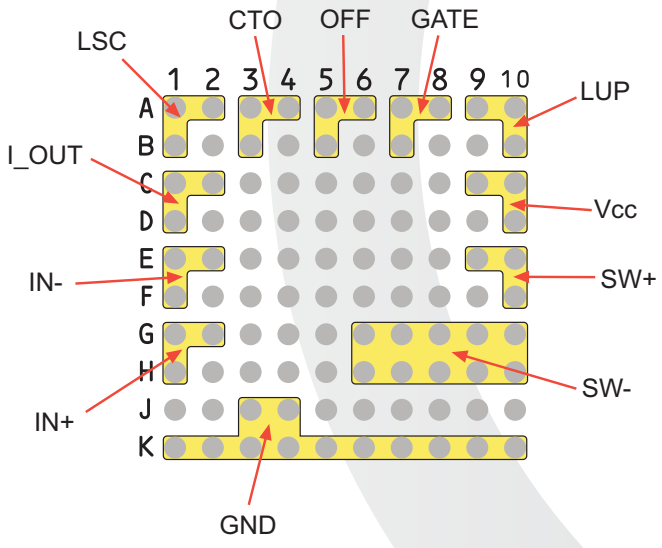
PINS DESCRIPTION

PIN Name	Documentation
GND	GROUND pin for the device
GATE	OUTPUT: to be connected to the gate of the external PMOS transistor, when used. It is also used to connect an optional external capacitor to limit slew-rate of the **SW-** pin. It can also be used to connect an optional external resistor to reduce slew-rate.
LSC	POWER: load sink. Sinks a current from load during a latchup condition.
VAL	SUPPLY pin for the device
CTO	INPUT: positive terminal of capacitor to set the turn-on time. The other terminal should be connected to **LUP** pin.
SW-	POWER: negative side of load power switch. It should be connected to the load, except when an external PMOS transistor is used. It can also be used to connect an optional external capacitor to limit the slew-rate of the **SW-** pin.
SW+	POWER: positive side of load power switch. It should be connected at the negative side of external shunt resistor, except when an external PMOS transistor is used
LUP	OUTPUT: set at logic-1 when a latchup or overload condition has been detected. Remains high for the whole turn-on time. Logic-1 level is coincident with supply voltage. It can also be used to connect an optional external capacitor to set the turn-on time.
I_OUT	OUTPUT: Ground-referenced voltage proportional to the load current. When load power is turned off due to a latchup or overload condition, output voltage is unpredictable. It can also be used to connect an optional external capacitor to set the **allowed inrush current.**
OFF	INPUT: load enable. When at logic-1 enables load power supply. When al logic-0 turns load power off
IN-	INPUT: negative side of external shunt resistor. It should be connected to the Load via the Power Load Switch.
IN+	INPUT: positive side of external shunt resistor. It should be connected to power supply generator.

PINS LAYOUT (Top View)



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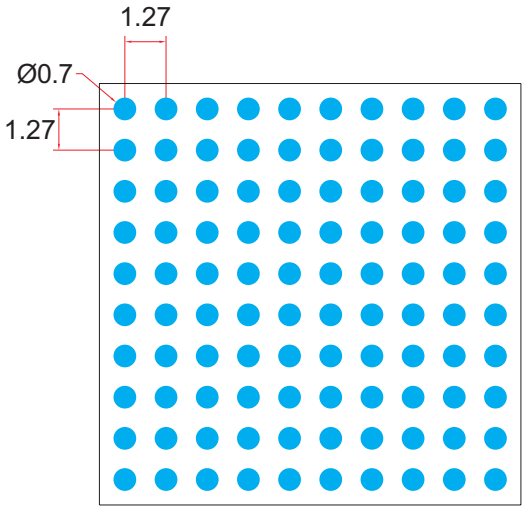
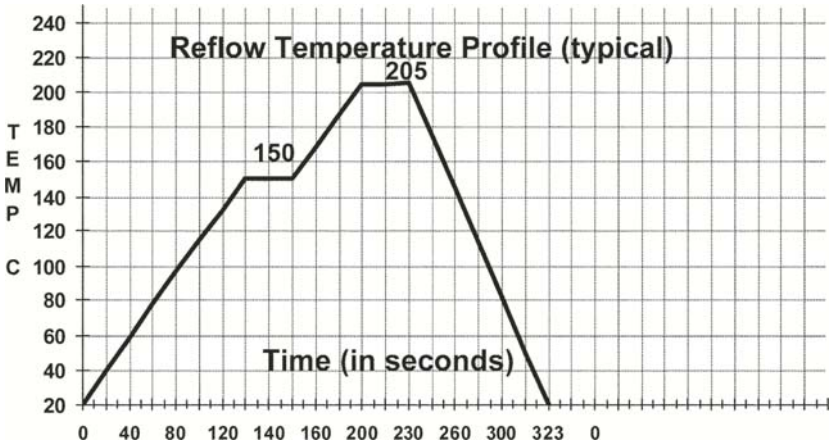
SOLDERING PATTERN



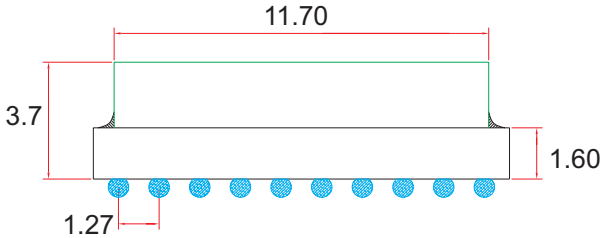
SOLDERING PRECAUTIONS

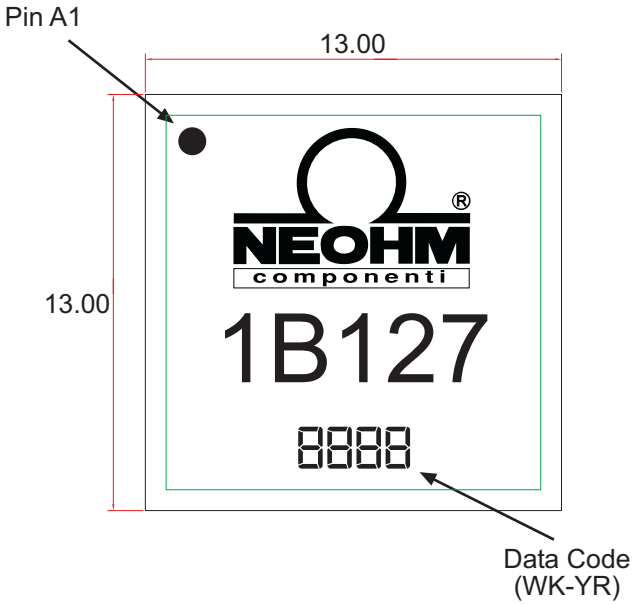
Before soldering put the 1B127 in oven @ 50° for 30 minutes



PACKAGE OUTLINE

(All dimensions are in mm)





ESD SENSITIVITY

The device can be damaged by ESD: we suggest to handle all integrated circuits with appropriate precautions.

Total or partial failure of the system can be originated by wrong installation and handling procedures.

ACKNOWLEDGEMENTS

This device has been designed in cooperation with the Space Avionics Technology Center of Dept. of Electronics of Politecnico di Torino, and is supported by project MAESS funded by Regione Piemonte (I).

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